REMARKS

Claims 1-18 are currently pending in this application. Claims 1-2, 4-6, 8-9, 11-13 and 15 have been rejected under 35 USC §102(b) as being anticipated by Vishakhadatta et al. (US Pat. No. 6,111,712). Favorable reconsideration and further examination are respectfully requested.

Claims 16-18 have been allowed. Claims 3, 7, 10 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Claims 1-18 are amended herein, with claims 3, 7, 10 and 14 being rewritten in independent form. The allowed claims, claims 16-18, have been amended, but the substance of the claims remains unchanged. Thus, claims 16-18 are still patentable over the prior art and are not further discussed herein.

Amended independent claim 1 recites, *inter alia*, a clock system including a reference clock for generating a first clock signal of a first frequency, control circuitry for generating a sync signal, the sync signal being associated with a reference edge of the first clock signal, clock modules respectively disposed on electronic assemblies, the clock modules including synthesizer circuitry for generating at least one second clock signal having one or more second frequencies, wherein at least one of the second frequencies is different from the first frequency and fanout circuitry coupled to the reference clock and the clock modules to distribute the first clock signal and the sync signal.

Amended independent claim 8 recites, *inter alia*, a frequency-based semiconductor tester including reference clock circuitry for generating a first clock signal of a first frequency, control circuitry for generating a sync signal, the sync signal being associated with a reference edge of the first clock signal, clock modules having synthesizer circuitry for generating at least one

second clock signal having one or more second frequencies, wherein at least one of the second frequencies is different from the first frequency, and fanout circuitry coupled to the synthesizer circuitry and the reference clock circuitry for distributing the first clock signal as a reference signal for the synthesizer circuitry and the sync signal.

Amended independent claim 15 recites, *inter alia*, a method of clocking including generating a first clock signal of a first frequency, generating a sync signal, the sync signal being associated with a reference edge of the first clock signal, distributing the first clock signal and the sync signal to clock modules disposed on electronic assemblies and generating at least one second clock signal with the clock modules, at least one of the second clock signals having one or more second frequencies wherein at least one of the second frequencies is different from the first frequency.

Independent claims 1, 8 and 15 are patentable over Vishakhadatta et al. because the reference does not show or suggest a clock architecture and method for distributing a digital clock signal including, *inter alia*, reference clock circuitry for generating a first clock signal, control circuitry for generating a sync signal, the sync signal being associated with a reference edge of the first clock signal, clock modules having synthesizer circuitry for generating one or more second clock signals, and fanout circuitry coupled to the synthesizer circuitry/clock modules to distribute the first clock signal and the sync signal.

Vishakhadatta et al. teach a system and method to improve the jitter performance of high frequency synthesizers used in read/write channel circuits. The frequency synthesizer has multiple phase locked loops arranged in a cascaded fashion to increase the update rates at which the cascaded loops operate at for a given frequency resolution of the synthesizer. *See* abstract.

Vishakhadatta et al. disclose that the frequency synthesizer includes two or more phase lock loops (PLLs) provided in series. *See* Fig. 4; col. 7, lines 56 – 57 ("The output 417 of PLL 1 404 is provided as an input to PLL2 406."); Fig. 5; col. 9, lines 26 – 30 ("The frequency synthesizer 500 includes one first stage PLL1 404 and three second stage PLLs-PLL2A 406A, PLL2B 406B, and PLL2C 406C which each receive the output of the first stage PLL1 404 for use as a input clock signal.") The present invention does not disclose or suggest that PLLs be provided in series and does not disclose or suggest that the output of one PLL be provided as the input to another PLL.

In addition, Vishakhadatta et al. do not show or suggest a system and method that includes a first clock signal and a sync signal, wherein fanout circuitry coupled to a reference clock and clock modules having synthesizer circuitry distribute the first clock signal and the sync signal. For the foregoing reasons, independent claims 1, 8 and 15 are patentable over Vishakhadatta et al.

Dependent claims 2-7 and 9-14 depend directly or indirectly from independent claims 1, 8 and 15 and thus contain all of the limitations of the independent claims from which they depend. Therefore, these dependent claims are patentable over Vishakhadatta et al. for at least the same reasons set forth above with respect to claims 1, 8 and 15.

The amendment to the specification corrects a typographical error found on page 7, line 10 of the application. The paragraph has been amended to correctly identify the reference numeral for clock module 40. No new matter has been added.

Enclosed is a Petition for a Two Month Extension of Time. Please charge the required fee to Deposit Account No. 20-0515, Docket No. 1466-US.

Applicants submit that all of the claims are now in condition for allowance, which action is requested. Please apply any additional charges or credits to Deposit Account No. 20-0515.

Respectfully submitted,

Kathryn E. Noll

Kathryn E. Noll
Reg. No.: 48,811
Attorney for Applicants

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Teradyne, Inc.
321 Harrison Avenue, MS-H61
Boston, MA 02118
Telephone: (617) 422-2676
Facsimile: (617) 422-2290